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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,401	12/28/2001	Yat-Tung Lam	MP0056.C1	4485

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EXAMINER	
RODRIGUEZ, GLENDA P	
ART UNIT	**PAPER NUMBER**
2627	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,401	LAM, YAT-TUNG	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-12, 14-19, 21-28, 30-35, 37-38* is/are rejected.

7)☒ Claim(s) *7,13,20,29 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 14, 8, 23, 30, 2, 15, 24, 31, 6, 12, 19, 28, 35 rejected under 35 U.S.C. 102(e) as being anticipated over (US Patent No. 6, 522, 608) to Kuroda.

Regarding Claims 1 and 14, Kuroda teaches a read circuit which provides multi-bit disk data to a disk controller based on analog data from a disk head, said read circuit comprising:

A bit detector for providing single bit digital data corresponding to the analog data from the disk head, the bit detector being synchronized by a high frequency clock (See Col. 7, L. 60-62, wherein it teaches the PLL circuit 70 receiving a signal and outputs a synchronizing clock. It is very well known in the art that a clock consists of "1" and "0" bits, hence providing a single data bit. It is also known in the art that all clocks are high frequency clocks.);

A synchronization mark detector for detecting a synchronization marker in response to said but detector (Element 69); and

A clock generator for generating a lower- frequency clock from the high frequency clock with a phase adjustable in response to the synchronization mark detector (See Figs. 10 and 11 along with Col. 2, Element 26-65 and Col. 14, L. 40 to Col. 15, L. 24, wherein Kuroda teaches that the clock signal is being adjusted

according the synch signal found in a synch data or marker detection and the phase is adjusted by changing the clock (either to a lower frequency or a higher frequency) in order to produce synchronization in the signal).

Method claims (8) is drawn to the method of using the corresponding apparatus claimed in claims (1 and 14). Therefore method claim (8) corresponds to apparatus claim (1 and 14) and are rejected for the same reasons of anticipation as used above.

Claims (23 and 30) have limitations similar to those treated in the above rejections, and are met by the references as discussed above. Claims (23 and 30) however also recite the following limitations: "a disk head (Element 60) and a disk controller (or processor Element 9)."

Regarding Claim 2, 15, 24 and 31, Kuroda teaches all the limitations of Claims 1, 14, 23 and 30, respectively. Kuroda further teaches wherein said synchronization mark detector detects the synchronization marker based on the single bit data from said bit detector (Col. 6, L. 57-65).

Regarding Claim 6, 12, 19, 28 and 35, Kuroda teaches all the limitations of Claims 1, 8, 14, 23 and 30, respectively. Kuroda further teaches wherein clock generator counts a high frequency clock and adjusts phase of the lower-frequency clock by a reset of the count (Col. 11, L. 45 to Col., 12, L. 14, wherein Kuroda teaches that the clock frequency is changed and it is then reset.).

5. Claims 3-5, 9-11, 16-18, 25-27, 32, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Vishakadatta et al. (US Patent No. 6, 111, 712).

Regarding Claims 3, 9, 16, 25 and 32, Kuroda teaches all the limitations of Claims 1, 8, 14, 23 and 30, respectively. However, Kuroda does not explicitly teach wherein said high frequency clock is phase-locked to output of the disk head. Vishakadatta et al. teaches this

limitation in the Summary of the Invention wherein it has a frequency synthesizer in which more than one PLL, all with different clock frequencies, can be chosen. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Kuroda's invention with the teaching of Vishakadatta et al. in order to be able to operate at different rates for a given frequency as described in the Summary of Vishakadatta et al.

Regarding Claim 4, 10, 17, 26 and 33, Kuroda teaches all the limitations of Claims 1, 8, 14, 23 and 30, respectively. However, Kuroda does not explicitly teach further comprising an A/D converter for converting the analog data from the disk head to multi-bit digital data and providing such multi-bit digital data to said bit detector (Element 320).

Regarding Claim 5, 11, 18, 27 and 34, the combination of Kuroda and Vishakadatta et al. teach all the limitations of Claims 4, 10, 17, 26 and 33, respectively. The combination further teach wherein said A/D converter operates in synchronism with said high frequency clock (See Fig. 1, Element 354, wherein the clock is also sent to the ADC).

6. Claims 21, 22, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda in view of Uno (US Patent No. 6, 301, 066).

Regarding Claim 21, 22, 37 and 38, Kuroda teaches all the limitations of Claims 1, 14, 23 and 30, respectively. However, Kuroda does not explicitly teach a high frequency clock, even though it is obvious to an artisan that if a clock varies according to the data, one of the frequencies must be the highest, thereby being a high frequency clock while reading certain data. Uno teaches a high frequency clock in Col. 12, L. 36-43). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Kuroda's

invention with the teaching of Uno in order to process parallel data at high speed as taught by Uno in the Summary of the Invention.

Allowable Subject Matter

7. Claims 7, 13, 20, 29 and 36 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The reasons for allowance are cited in the previous Office Action dated 02/06/06.

Response to Arguments

8. Applicant's arguments filed 5/01/06 have been fully considered but they are not persuasive. Applicant's argue that "Kuroda does not show a bit detector providing a single bit corresponding to the analog data from the disk head and a synch mark detector for detecting a synchronization marker in response to the bit detector". Examiner does not concur with the Applicant. Due that the PLL circuit accepts the analog data provided by the read/write device, it the extracts single bits corresponding to a synch clock, and the synch mark detector, at the same time detects the synch marks and provides such information to the s/h timing generating circuit in order to improving the detection of the data. Hence, Kuroda teaches the limitations of the independent Claims and the rejection stands as cited.

9. Examiner acknowledges that the Terminal Disclaimer has been filed on 05/24/06.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gpr
07/24/06.

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER